Tektronix®

Signal Integrity Backplane Testing

APPLICATION NOTE

Introduction

As High-Speed-Serial (HSS) communication channels scale up to multiple lanes and faster bit rates, ensuring hardware interoperability becomes increasingly more complex. Impairments introduced at the backplane from module loading must be verified at the system level using a calibrated measurement system. Special consideration must be given to the test setup in order to improve the interoperability of modules inserted across the host backplane. For example, considerations must be made for modules and the backplane both together and separately as connected in the system. This discussion will address HSS signal considerations associated with the backplane channel.

Discussion

- Backplane Considerations
- Backplane Signal Payload and Signal Coupling
- Test Point Designations
- Test Platform Calibrations
- Loss Models and Budgets
- Probe/Cable Interconnect
- Embedding/De-Embedding
- Jitter and Noise Analysis
- Victim/Aggressor Analysis

Backplane Considerations

Modern backplanes can be verified by making physical signal measurements or by simulating the channel operating margin (COM). Here we will focus on considerations for verifying a backplane by making physical signal measurements at multiple test points of the system. These measurements should be made at both the near end and far end of the signal chain, with channel paths being represented as a composite of all channel paths between the transmitter and receiver end points.

It is recommended to measure the backplane channel separately to verify Insertion Loss, Continuity, Reflections, and Crosstalk. Also, when performing a system-level test, the signal quality of each Plug-In-Card (PIC) should be verified against its specification before being inserted into the backplane.

Factors that must be verified:

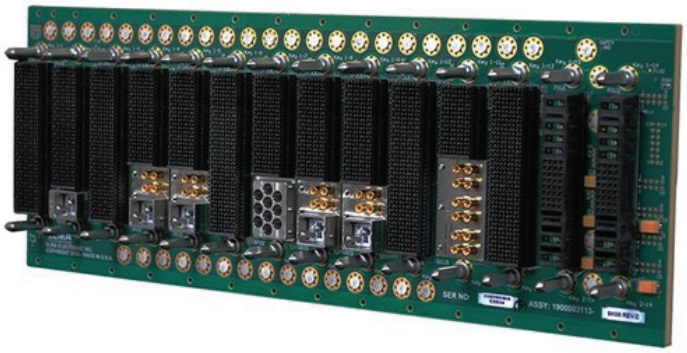
- Loss budget specification for each backplane channel (losses will vary)
- Impairments caused by discontinuities in channel traces and interconnections
- Crosstalk caused by Victim/Aggressor Coupling on adjacent traces and planes
- Jitter and noise characterization of signal (SDLA will allow measurement at each test point given S-parameters without moving probe point)
- Jitter and eye testing using stressed signal patterns
- Calibrated measurement system with proper backplane isolation

Module and backplane considerations:

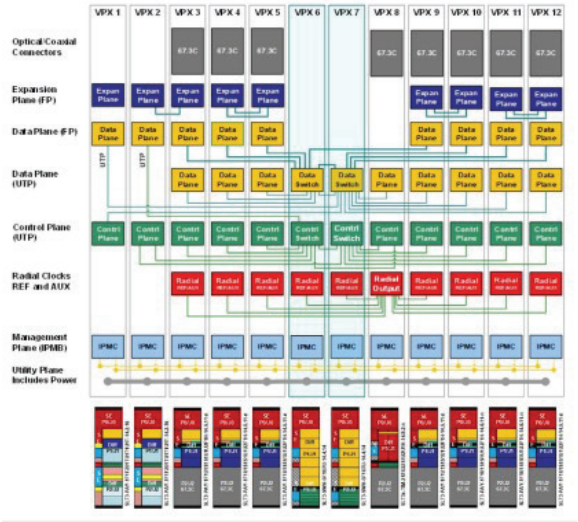
- Characterize the backplane prior to inserting the PIC
- Measure the loss budget using calibration fixtures with the proper adaptor interconnects to break out the signals
- Use breakout boards (also called “Paddle Cards”) to measure the signal transmission from the PIC across the backplane at the designated test points

Backplane Signal Payload Mapping and Signal Coupling

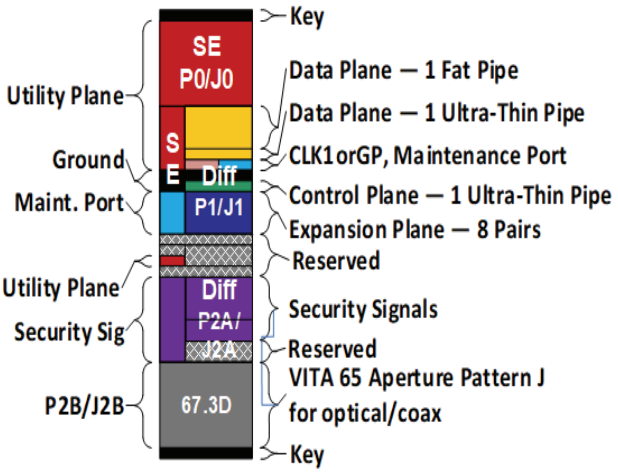
Typically, a backplane is expected to support both commercial off-the-shelf (COTS) and proprietary PICs in a single system. However, in a distributed backplane architecture, HSS signals are subjected to signal impairments such as channel loss, imperfect signal coupling, and module loading return loss. Additionally, each module will have electrical signals with both high and low power operation requirements. Supporting mixed-mode channels and groupings such as RF and optical standards in the same backplane presents even more challenges.



Backplane configurations vary significantly in size and function. Often, mixed signals must be managed for proper function across the backplane. HSS signals are susceptible to crosstalk, EMI, and other forms of coupling. Proper module layout is a critical consideration for ensuring interoperability by maintaining proper channel loss budgets.



Structured signal group mapping and layout of a mixed-signal backplane architecture showing backplane buses, discrete signals, and power/ground planes.



Connector layouts define the type of PIC supported by a particular backplane connector. To ensure proper interoperability, the combined channel loss of the backplane and PIC must not exceed the total loss budget of the channel. For this reason, additional consideration must be given for PICs with HSS buses regarding backplane slot placement

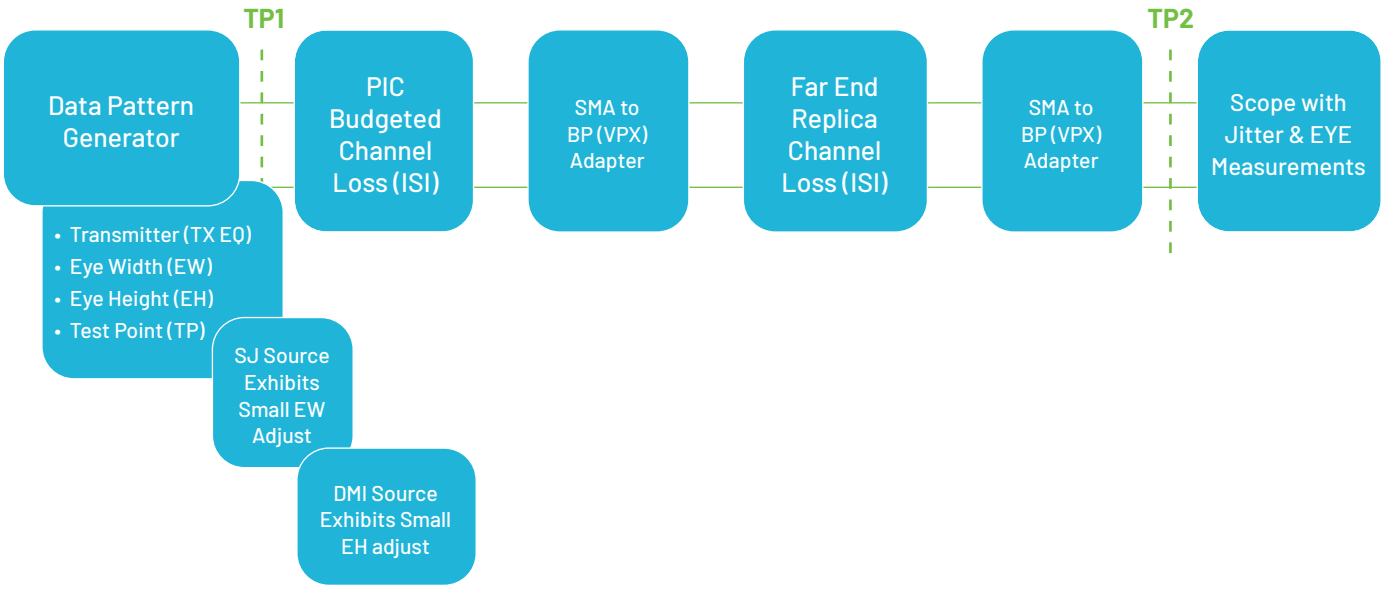
Test Point Designations

To ensure accurate results when measuring HSS signals, a calibrated measurement system must be used to measure the signal at the designated test points. The measurement system should include the proper interconnect adapters, ISI loss fixtures, and replica channels.

- TP1 is connected directly to the scope for measurements in calibration
- The pattern generator will transmit test patterns such as compliance, PRBS, or custom, having varied stresses at amplitude that will need to be calibrated for correct stress impairments - needed for transmit equalization requirements in test specification
- Random and sinusoidal (adjustment for EYE width) jitter impairments
- Combiner is used to inject differential mode (adjustment for EYE height) and common mode interference
- TP2 signal is measured at far end of backplane channel to scope, allowing for full channel stress measurements
- TP2 signal injection to backplane at near end
- Calibration channel loss compensated
- Replica channel loss compensated

Calibration Result

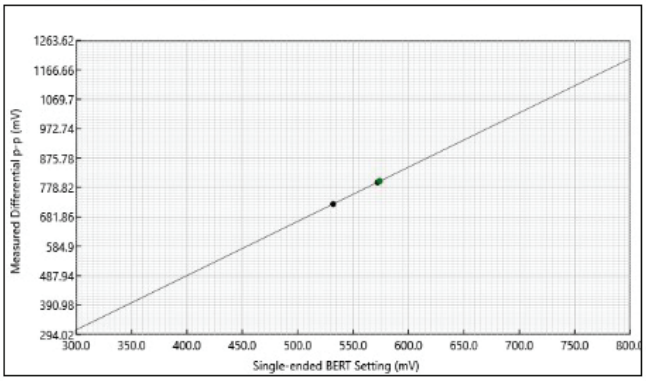
- Compensate for the actual loss in the signal path
- Compensate for RJ and SJ impairments in the HSS test pattern
- Use transmission channel equalization to compensate for the stress signal EH and EW



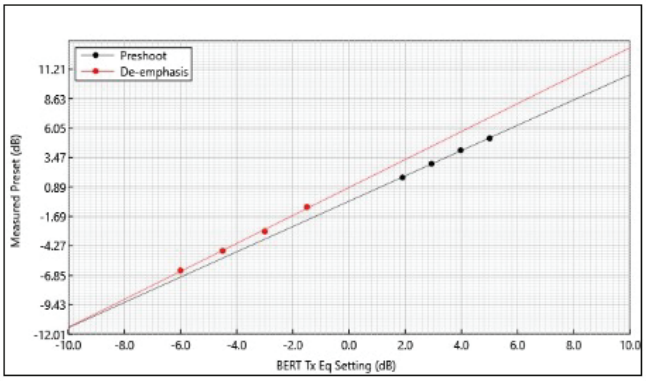
Test Platform Calibrations TP1 (example plots)

TP1 calibrations are needed to compensate for signal amplitude loss from the data generator to ISI loss fixture as well as the Rj and Sj sinusoidal jitter profile. These calibrations will be used to compensate the pattern generator output levels for loss to injection point at TP1.

TP1 Calibration Details	
AC-DC Balance	Setting De-emphasis: 0 dB
	Pattern: 64ones_64zeros_128bit10
	Important RT Scope Settings: BW: 25.0 GHz, Sample Rate: 100.0 GS/s, Record Length: 5000
Amplitude Calibration	Setting: 574 mV (Nominal - 800.0 mV)
	Pattern: 64ones_64zeros_128bit10
	Amplitude Regression Line Parameters: Slope= 1.788, Intercept= -226.901



Preset Calibration	Pattern: 64ones_64zeros_128bit10
	Important RT Scope Settings: BW: 25.0 GHz, Sample Rate: 100.0 GS/s, Record Length: 5000
	De-emphasis Regression Line Parameters: Slope = 1.225, Intercept = 0.85
	Preshoot1 Regression Line Parameters: Slope = 1.109, Intercept = -0.35

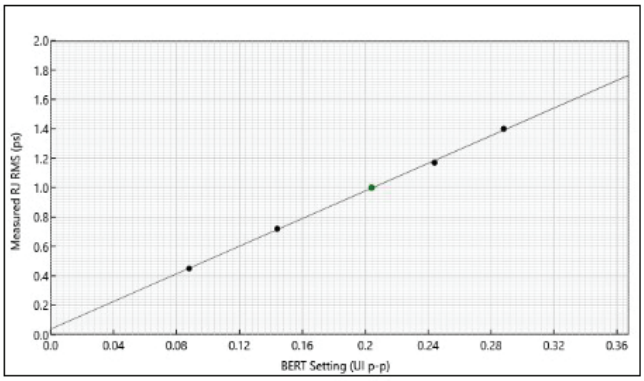


Amplitude calibration is required to compensate for variations in the generator output voltage due to changes in channel loss and data pattern. Compliance patterns improve consistency of measurement result. TX equalization presets are calibrated and prepare the signal for expected channel degradation.

TX equalization presets are calibrated and prepare the signal for expected channel degradation.

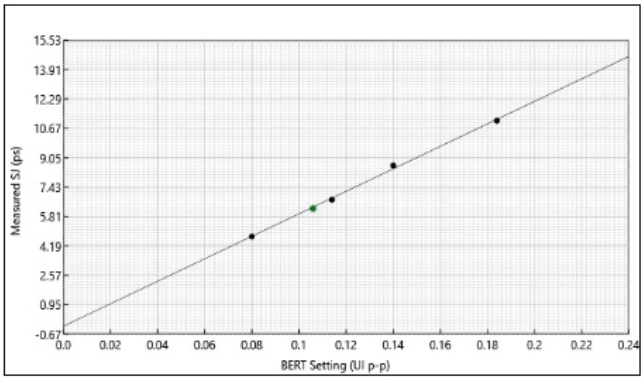
Test Platform Calibrations TP1 (example plots)

TP1 Calibration Details	
RJ Calibration	Setting: 0.204 UI p-p (Nominal - 1.0 ps RMS)
	Pattern: Toggle_1bit
	Important RT Scope Settings: BW: 25.0 GHz, Sample Rate: 100.0 GS/s, Record Length: 12500000
	RJ Regression Line Parameters: Slope = 4.698, Intercept = 0.038



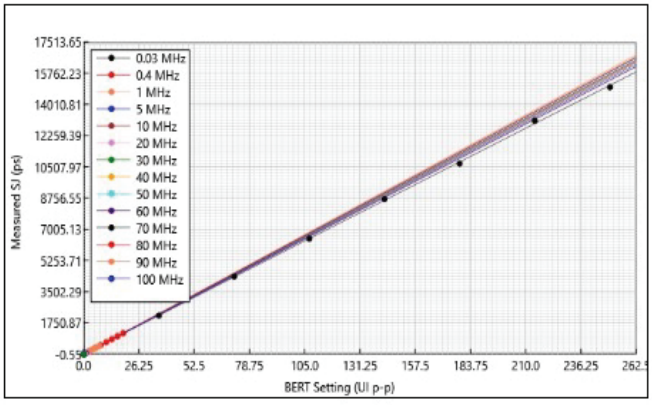
Random jitter (Rj) is injected into data pattern deterministically to understand system's sensitivity to random (unbound) jitter.

SJ Calibration	Setting: 0.106 UI p-p (Nominal - 6.25 ps)
	Pattern: 128b130b_CP_L0_Gen4_P7
	Important RT Scope Settings: BW: 25.0 GHz, Sample Rate: 100.0 GS/s, Record Length: 12500000
	SJ Regression Line Parameters: Slope = 61.972, Intercept = -0.236



Sinusoidal jitter (Sj) and sometimes a simple pattern excited jitter are also injected into data pattern deterministically to understand system's sensitivity to bounded jitter.

Multi-tone SJ	Calibration performed for 14 frequencies
	Pattern: 128b130b_CP_L0_Gen4_P7

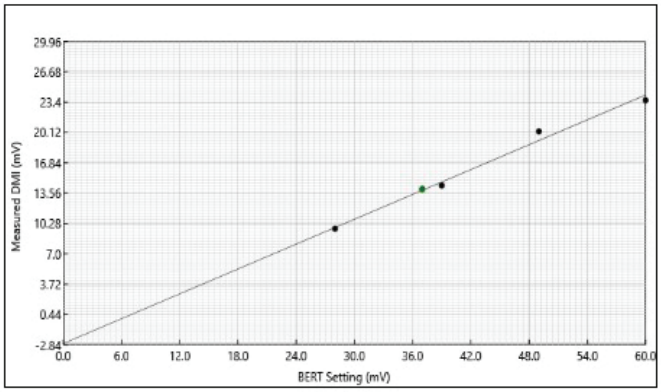


Multi-Tone SJ is used to test receiver's clock recovery jitter tracking (PLL loop bandwidth, etc.) at specified frequencies.

Test Platform Calibrations TP2 (example plots)

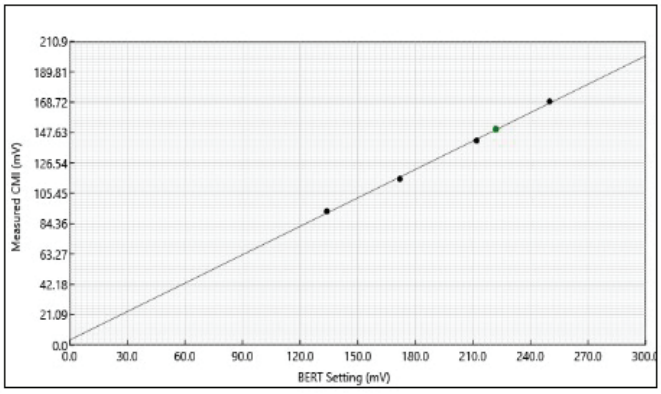
TP2 calibration provides a methodology to include Differential Mode Interference (DMI) and the Common Mode Interference (CMI) equivalents needed to model system cross talk.

TP2 Calibration Details	
DMI	Setting: 37 mV @ 2.1 GHz (Nominal - 14.0 mV)
	Pattern: Electrical_Idle
	Important RT Scope Settings: BW: 25.0 GHz, Sample Rate: 100.0 GS/s, Record Length: 4000
	Regression Line Parameters: Slope = 0.448, Intercept = -2.706



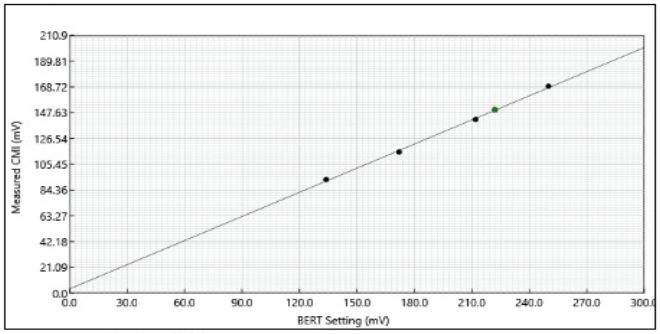
DMI is measured on channel with known loss representing the physical channel. ISI/DMI/SJ are used together to set EH &EW deterministically.

CMI	Setting: 222 mV (Nominal - 150.0 mV)
	Pattern: Electrical_Idle
	Important RT Scope Settings: BW: 25.0 GHz, Sample Rate: 100.0 GS/s, Record Length: 12500000
	Regression Line Parameters: Slope = 0.658, Intercept = 3.493



CMI is measured on channel with known IL loss representing the physical channel.

Test Platform Calibrations TP2 (example plots)

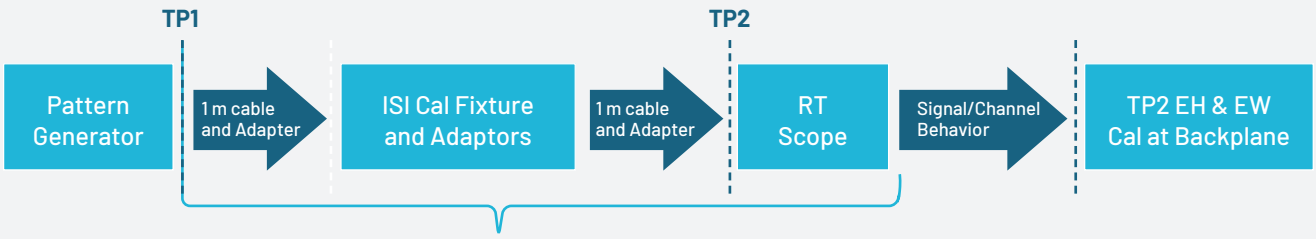
TP2 Calibration Details	
	
CTLE and Preset Selection	Selected Preset: P5
	Selected CTLE: 9.0
	Important BERT Settings: DMI: 37 mV @2.10 GHz, RJ: 0.204 UI p-p, SJ: 0.106 UI p-p, Pattern: 128b130b_CP_L0_Gen4_P7
	Important RT Scope Settings: BW: 25.0 GHz, Sample Rate: 100.0 GS/s, Record Length: 12500000

TX Equalization: CTLE (Signal Emphasis/Deemphasis) Preset			**Pattern Generator Settings: DMI: 37mv@2GHz, RJ:.20UI, SJ:.10UI, Pattern: PRBS15**		
RT Scope Settings:			BW: 20GHz, Sample Rate 100GS/s Record Length: 125M		
Index	**PE/DE Preset**	**CTLE**	**Eye Width (ps)**	**Eye Height (mv)**	**Eye Area**
1	P4	6	50.025	79.50	880.141
2	P4	6	50.050	80.00	807.663
3	P4	6	50.75	80.50	805.521

Signal emphasis/deemphasis allows for TX equalization to signal at TP1 & TP2 (calibrated response in channel) needed to open signal EYE for appropriate test pattern specified for HSS signal testing.

Calibrated Fixture Summary

The TP1 Cal is used to calibrate TP2 stresses with known channel loss to understand CMI and DMI. Apply SJ and DMI response to stressed data pattern such that EH and EW is appropriate for channel.

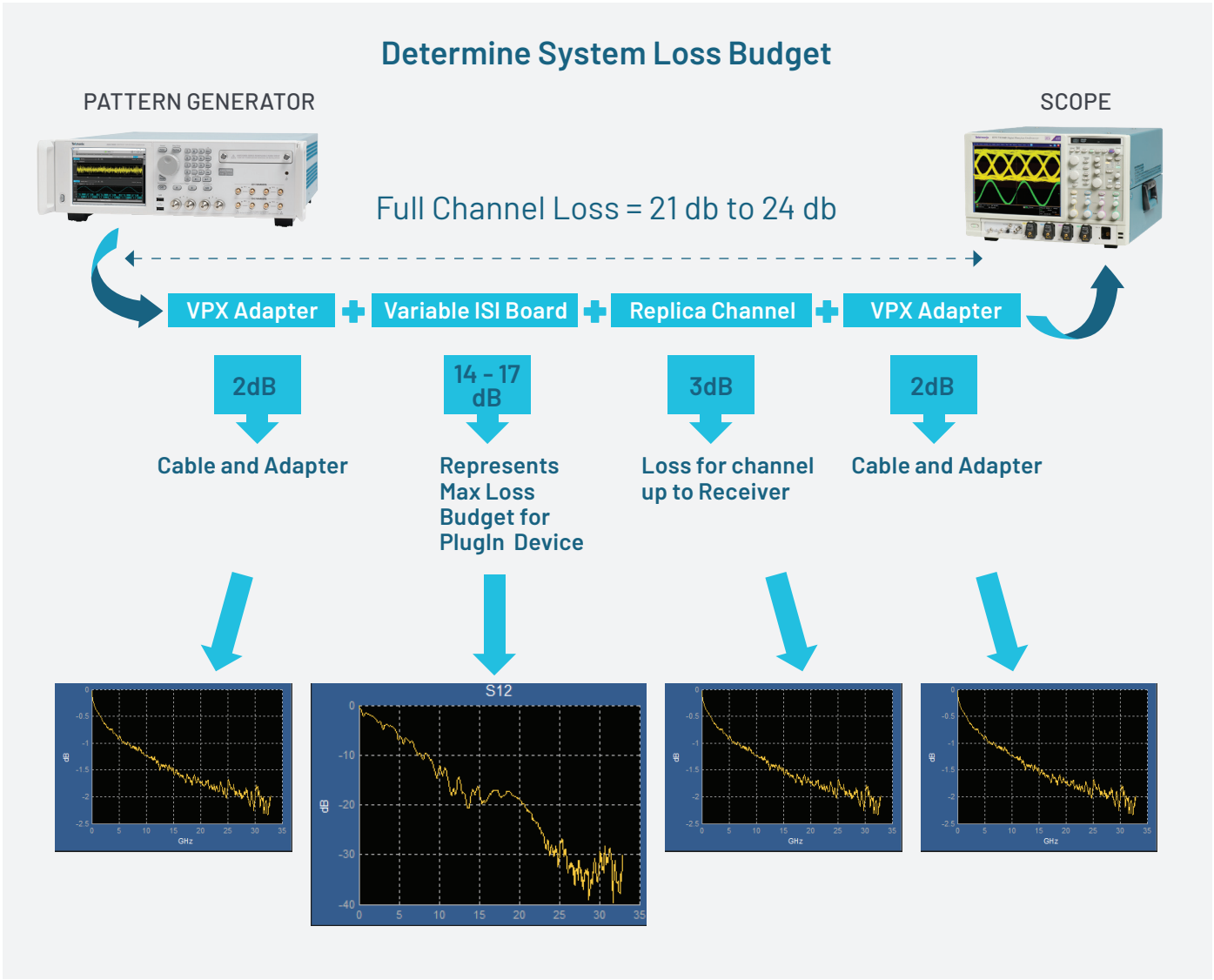


Specified dB Insertion Loss (IL for TP2 CMI/DMI) Budget for PIC in System

Calibration Summer	
TP2 Calibration	Unique ID: [Example_TP2_RC_Calibration]
	Full Channel Loss: 28.982 dB, Loss Mode: Manual
	DMI/CMI Loss: 23.72 dB
	Selected Preset: P5
	Selected CTLE: 9.0 dB
	ISI Pair: Pair 2 and 8
	Status: Converged
	Final Calibrated EW: 19.0 ps (18.25 ps ≤ Target EW ≤ 19.25 ps)
	Final Calibrated EH: 16.5 mV (13.5 ≤ Target EH ≤ 16.5 mV)
	Final SJ Stress Level: 6.75 ps / 0.114 UI p-p BERT Setting (5 ps ≤ SJ Sweep ≤ 10 ps)
	Final DMI Stress Level: 25.0 mV / 62 mV BERT Setting (10 mV ≤ DMI Sweep ≤ 25 mV)
	Final Amplitude Level: 800.0 mV (Differential) / 574 mV (Single-Ended) BERT Setting
	SJ@210 MHz Setting during JTOL test: 0.016 UI p-p
	(Calibrated Value of SJ (ps) required to achieve the target stressed eye width minus 6.25 ps)
	Final CMI Stress Level: 150.0 mV / 222 mV BERT Setting
TP1 Calibration	Unique ID: [Example_TP1_Calibration]
	Balanced De-emphasis: 0 dB
	Differential Amplitude: 800.0 mV / Single-Ended Amplitude Setting: 574 mV
	SJ Setting: 0.106 UI p-p @ 100 MHz (Nominal SJ 6.25 ps / 0.1 UI p-p)
	RJ Setting: 0.204 UI p-p (Nominal RJ 1.0 ps RMS / 0.016 UI p-p)
	SJ@210 MHz Regression Line Parameters: Slope = 64.892, Intercept = -0.555
	Multi-tone SJ Calibration performed for 14 frequencies

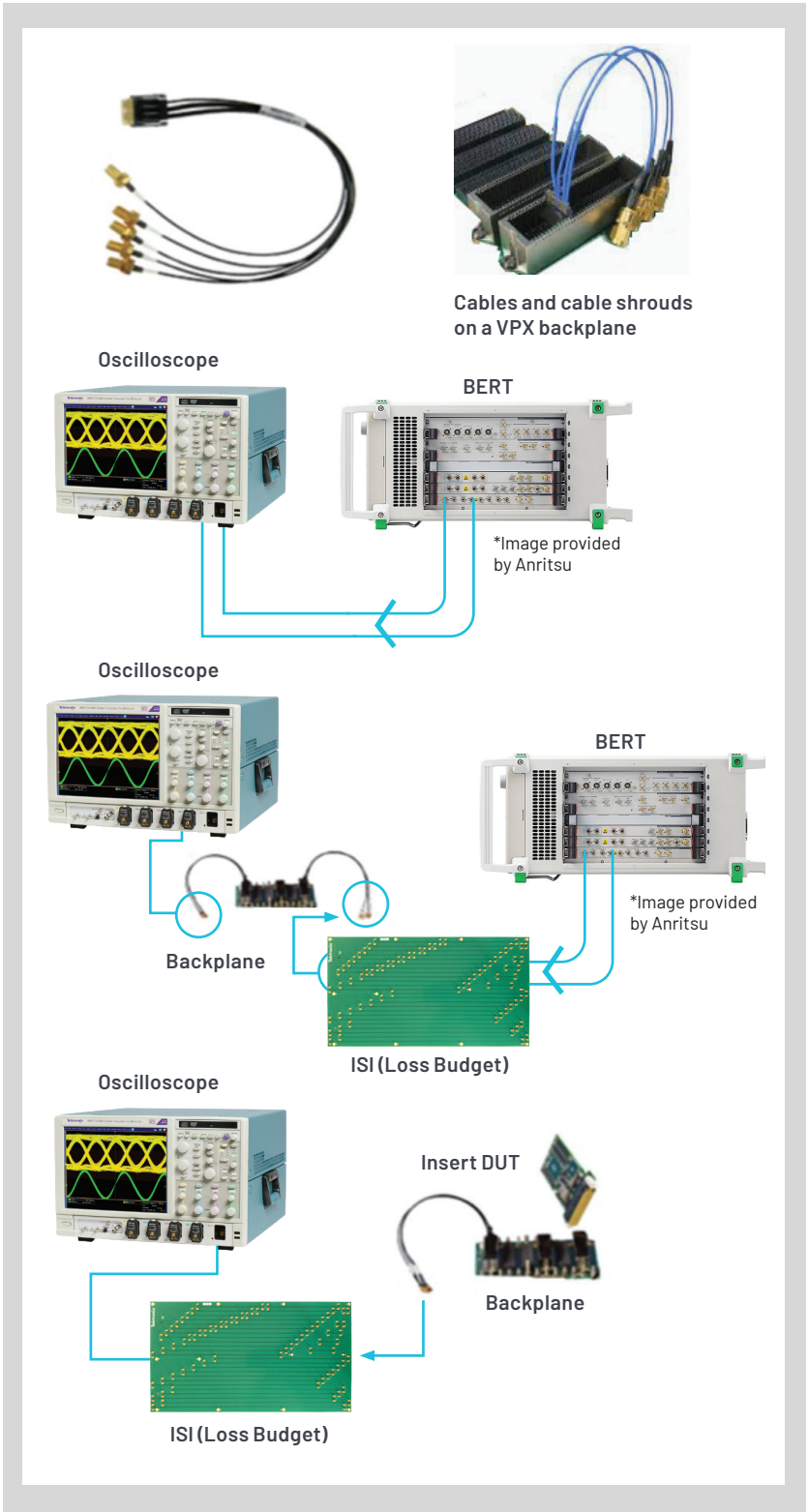
Loss Models and Budgets

Loss budgets are assigned to the physical channels representing the boundaries for the source card, backplane channel, and load card. Keep in mind every element in the signal chain will have a different package loss, so it is critical to test the PICs and backplane separately using a variable ISI fixture to establish the individual package losses and understand how they contribute to the maximum physical channel loss. HSS standards call for the maximum channel loss appropriate for calibrated data transmission. Interoperability is in jeopardy if any element of the transmission channel system exceeds the maximum specified loss budget.



Probe/Cable Interconnect

There are a variety of signal breakout adaptors available for COTS backplanes. These adaptors are used to connect test and measurement instruments, calibrated fixtures, and interconnect cables.



This is an example of SMA to VPX used to connect fixtures, cables, and instruments together.

TP1 example for calibration of data generator signal path injection.

Test case example for TP2 calibrated data generator signal path injection to backplane to measure SI.

Test case example for calibrated measurements from test module and backplane using loss budgeted measurements for SI.

Embedding & De-Embedding Channel Considerations

As serial communication channels scale up to multiple lanes and faster bit rates, measuring systems for ensuring compliance becomes increasingly complicated. Devices such as transmitters need to be verified to the package level, by measurement on a physical system.

Signal probing access directly at the measurement point in many cases is not possible and requires post-processing to remove channel impairments (de-embed) between the measurement point and test equipment. Measuring and de-embedding of the channel involves the use of S- Parameter Touchstone model of the passive system – the backplane and the interconnect around it. The S-parameters also can describe the crosstalk and inter-lane skew. Proper calibration of the instrumentation used and best techniques for probing in today's multi-lane channel should be done with care to avoid error or inaccuracies.

In the case of a multilane system, all traces must be characterized with TDR or a VNA. De-embedding is often needed as well. Frequently, the channel includes packages, connectors, and other structures that are difficult to model from separate s-parameter measurements, so emulating with a live transmitter waveform capture and s-parameters of the interconnect plus the channel is a good way to truly verify the channel. This example suggest that a combination of channel simulation and measurement can be used to accurately evaluate the system.

Often it is convenient to use physical S-parameter measurement for each component in sequence from near-end to far-end to define a composite model of the channel. Again, complete S-parameter matrix – S11, S21, S12 and S22 must be captured for every component. When the signal is measured at the near-end, and emulated with s-parameters to the far-end of the channel, the result will represent all impairments accordingly.

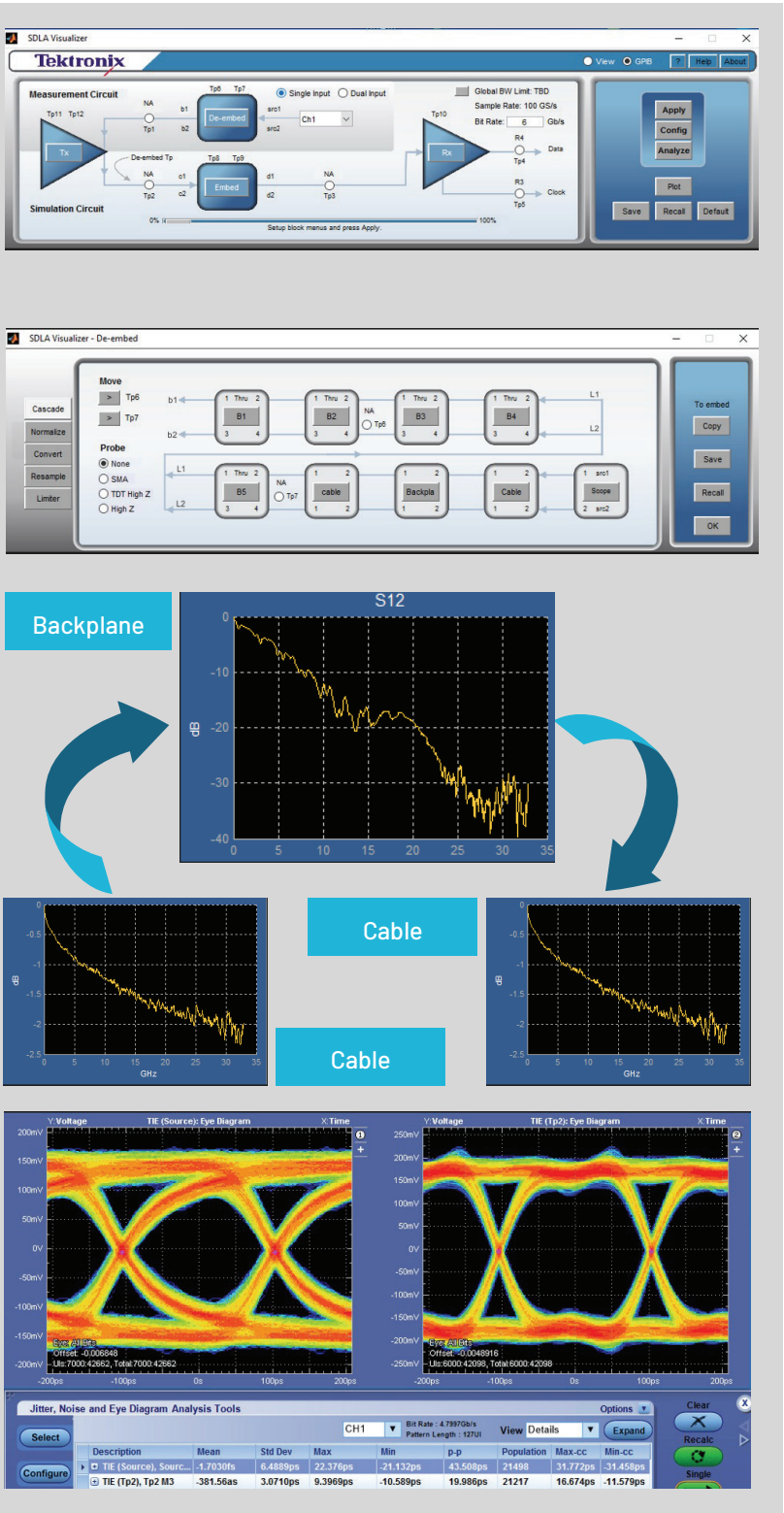
The purpose of de-embedding then is to capture the signal as it is at certain prescribed measurement points without the additional loss of e.g. the cable to the oscilloscope. The oscilloscope measures the signal at the end of the cable, and the impact of the cable can be de-embedded. The de-embedding effort is rewarded with a result that more closely matches the measurement test point. To perform de-embedding, all of the S-parameters should be accurately measured: the signal source's output s-parameters, the S22; the 4-parameter matrix of the cable, and the oscilloscope's S11, the input impedance. The interconnect to de-embed should be kept at minimum loss, since de-embedding is an imperfect tool and will add additional problems. Also, it is often valuable to consider IC package embedding parameters so that it is possible to effectively calibrate or test signals at the PADs within a package.

In the case of mid-channel measurement, any test point in sequence may be valid when the undesirable interconnects (e.g., oscilloscope cables) are properly de-embedded and parts of the channel that are not physically present are embedded carefully for the desired measurement.

Modeling tools such as Tektronix "SDLA" are available for use on oscilloscopes that use both physical and simulated parameters to model the signal path for measurement. Such modeling tools allow for source transmission equalization/ termination, channel embedding/de-embedding, and receiver equalization.

Embedding & De-Embedding Channel Examples Using SDLA

The SDLA tool creates, as its result, an oscilloscope filter. This filter is then applied to acquired waveforms to uncover the precise shape of the signal in the physical signal path. The filter compensates and emulates the waveform data to understand signal behavior in the physical signal path.



High speed signals can be characterized using modeling tools that utilize physical channel measurements.

Touchstone S-parameters of physical channel losses are used for embedding and de-embedding. De-embedding allows for removal of losses for unimpaired measurement. Embedding inserts losses in composite channel sequence allowing for desired test point measurement location.

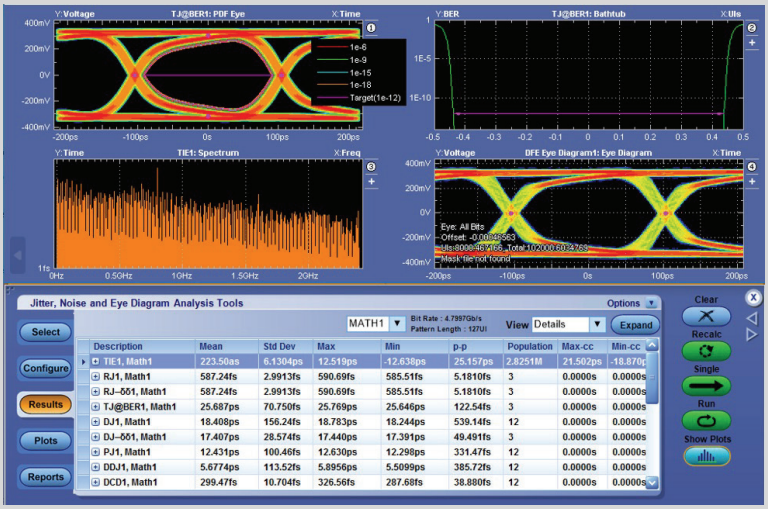
S-parameters may represent connectors, traces, discontinuity, or device losses that may be arranged to describe composite channel losses. Sequence in model allows for insertion of test points for measurement of channel.

HSS signal at far-end of channel is shown at left plot with all channel impairments.

Near-end of channel is shown at right plot. By de-embedding all channel losses, the source signal is represented without impairment at transmitter.

Jitter & Noise Analysis

HSS signal behavior can be characterized by measuring a known data pattern transmitted through the system's impaired physical channel. Jitter and noise will be represented in composition of signal impairments. Decomposition of jitter and noise will have known response signature that defines specific issues measured at the test point at the physical channel.

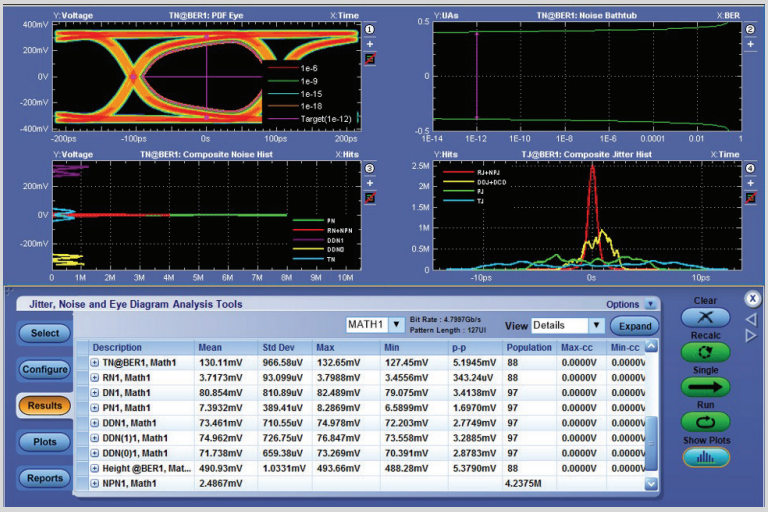


Total Jitter Summary Transitions

HSS signal with fixture and backplane showing jitter and noise measurements.

BER is represented at test point showing UI bit error depth relative to bathtub curve.

EYE diagrams are used to show EH & EW as well as many other impairments and measurements of merit (rise time, slew, etc.).



Total Noise Summary

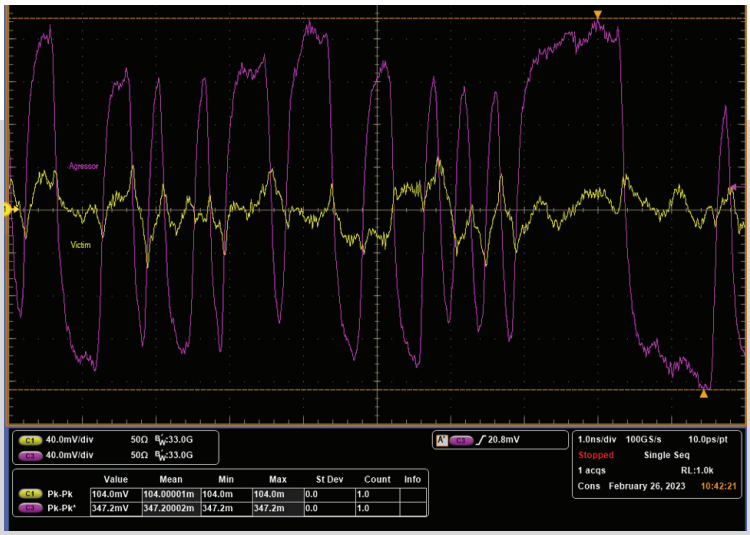
The noise bathtub curve shows variations in amplitude relative to noise present at the UI showing BER for noise.

Total jitter decomposition shows individual plots for each jitter contributor such as PJ, RJ, DCD, etc.

Total noise decomposition shows individual vertical plots for elements such as PN, RN, etc.

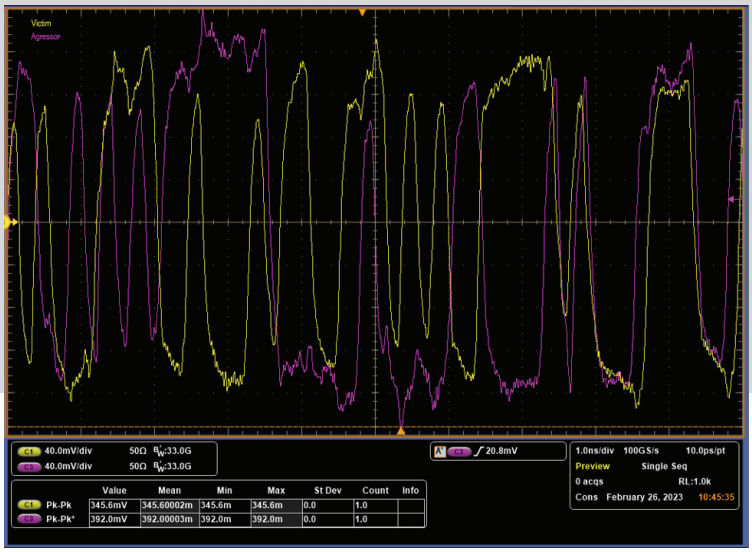
Victim/Aggressor Analysis

HSS with high channel counts are susceptible to coupling between channel paths. Signal fields are coupled from one trace to another when complete isolation is not possible in today's channel. Understanding crosstalk and other coupling sources is helpful to properly compensate/equalize data pattern transmissions. Also, it is important to use jitter and noise decomposition to understand possible sources of coupling behavior.



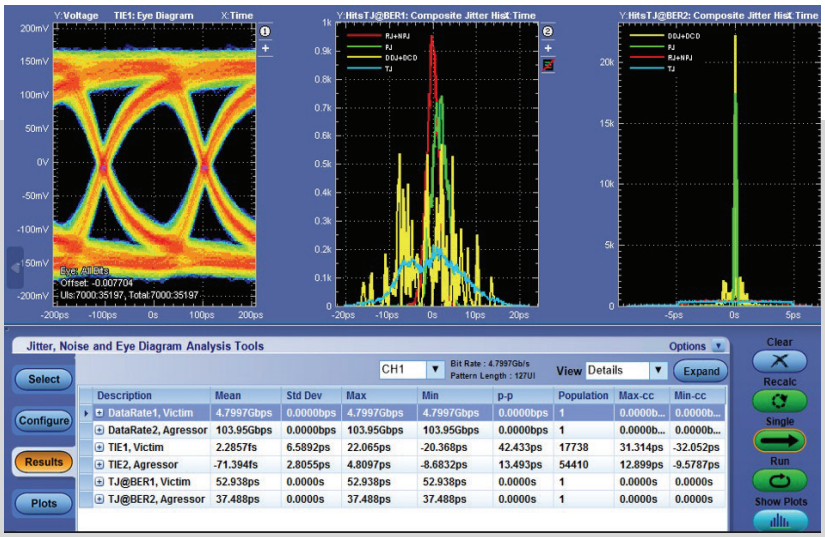
Victim channel inactive with active aggressor coupling on victim.

Victim/aggressor channels active coupling between both traces.



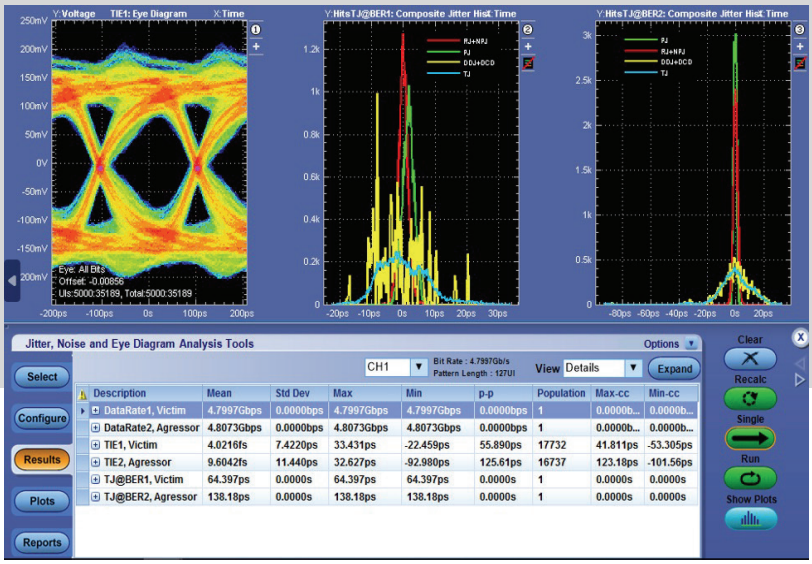
Victim/Aggressor Analysis (examples)

Below are victim EYE and jitter measurements for aggressor channel active on/off. This shows substantial victim channel impairments in the presence of the aggressor signal channel. Note in the bottom plot the increase in Rj and NPJ jitter results in the victim impairments decomposition, as well the impaired EYE is showing crosstalk coupling contributed by active aggressor.

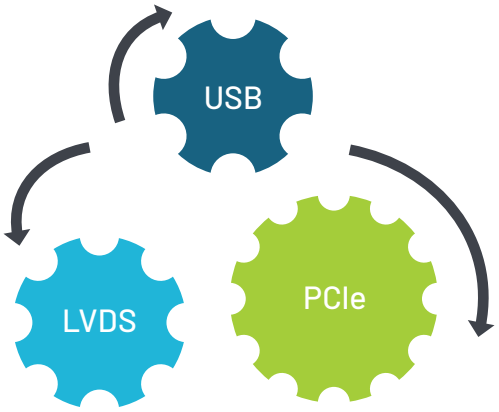


Victim EYE and jitter without aggressor

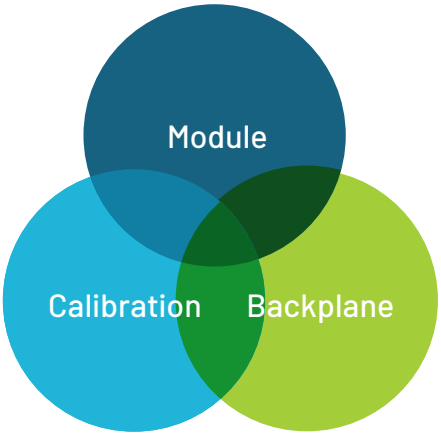
Victim EYE and jitter with aggressor



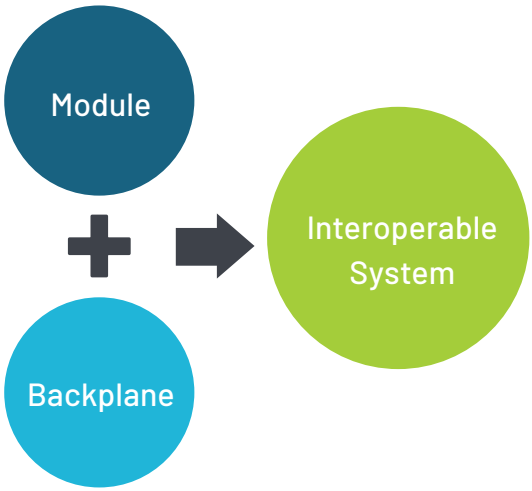
Key Findings



High-Speed-Serial (HSS) communication channels scale up to multiple lanes and faster bit rates, measuring systems to ensure interoperability become increasingly complicated.



Module loading introduces impairments at the backplane that need to be verified at the system level, by measurement on a calibrated measurement system.



There are considerations that should be applied to improve interoperability of modules inserted across the backplane. Such considerations must account for modules and backplane together and separately as connected in the system.

Conclusion

HSS signals from module to backplane will be impaired at the channel signal path. Calibrated test methodologies will enable proper compensations that allows for interoperability.

- Use calibrated test fixtures and observe channel loss budget in channel for signal compensation.
- Use embedding and de-embedding of signal channel to measure accurately at all test points without moving the probe.
- Crosstalk is possible both at the module and backplane, so it is best to characterize crosstalk separately, then as a system.

Contact Information:

Australia 1 800 709 465
Austria* 00800 2255 4835
Balkans, Israel, South Africa and other ISE Countries +41 52 675 3777
Belgium* 00800 2255 4835
Brazil +55 (11) 3530-8901
Canada 1 800 833 9200
Central East Europe / Baltics +41 52 675 3777
Central Europe / Greece +41 52 675 3777
Denmark +45 80 88 1401
Finland +41 52 675 3777
France* 00800 2255 4835
Germany* 00800 2255 4835
Hong Kong 400 820 5835
India 000 800 650 1835
Indonesia 007 803 601 5249
Italy 00800 2255 4835
Japan 81 (3) 6714 3086
Luxembourg +41 52 675 3777
Malaysia 1 800 22 55835
Mexico, Central/South America and Caribbean 52 (55) 88 69 35 25
Middle East, Asia, and North Africa +41 52 675 3777
The Netherlands* 00800 2255 4835
New Zealand 0800 800 238
Norway 800 16098
People's Republic of China 400 820 5835
Philippines 1 800 1601 0077
Poland +41 52 675 3777
Portugal 80 08 12370
Republic of Korea +82 2 565 1455
Russia / CIS +7 (495) 6647564
Singapore 800 6011 473
South Africa +41 52 675 3777
Spain* 00800 2255 4835
Sweden* 00800 2255 4835
Switzerland* 00800 2255 4835
Taiwan 886 (2) 2656 6688
Thailand 1 800 011 931
United Kingdom / Ireland* 00800 2255 4835
USA 1 800 833 9200
Vietnam 12060128

*** European toll-free number. If not accessible, call:** +41 52 675 3777

Rev. 02.2022

Find more valuable resources at TEK.COM

06/2023 SMD 64W-74004-0